

Amendments to the Claims

Claim 1: (currently amended) A method of fabricating an integrated circuit comprising the steps of:

forming a HDP (high density plasma) liner layer over a semiconductor body having metal leads formed thereon, wherein a portion of said HDP liner layer over said metal leads has sloped edges;

forming a gap-fill layer over said liner layer, said gap-fill layer filling a space between ~~closely-spaced ones of~~ said metal leads;

forming a dielectric layer over said gap-fill layer and said metal leads; and

forming a via through said dielectric layer to at least one of ~~said closely-spaced~~ metal leads.

6 Claim 2: (original) The method of claim 1, wherein said sloped edges have a slope on the order of 45°.

Claim 3: (original) The method of claim 1, wherein said dielectric layer comprises PETEOS.

-Claim 4: (original) The method of claim 1, wherein said dielectric layer comprises a silane based oxide.

Claim 5: (currently amended) The method of claim 1, wherein the portion of HDP liner layer over the metal leads is ~~approximately~~ triangular shaped.

Claim 6: (currently amended) The method of claim 1, wherein the portion of HDP liner layer over the metal leads is ~~approximately~~ trapezoidal.

Claim 7: (original) The method of claim 1, wherein said step of forming said HDP liner layer uses an etch-to-deposition ratio in the range of 0.18 to 0.40.

Claim 8: (original) The method of claim 1, wherein said HDP liner layer comprises undoped HDP silicon dioxide.

Claim 9: (original) The method of claim 1, wherein said HDP liner layer comprises fluorinated HDP oxide.

Claim 10: (original) The method of claim 1, wherein said HDP liner layer comprises phosphorous doped HDP oxide.

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Claim 11: (original) The method of claim 1, wherein said gap-fill layer comprises a spin-on glass.

Claim 12: (original) The method of claim 1, wherein said gap-fill layer comprises HSQ.

Claims 13-18 (cancelled).
